	TANTA UNIVERSITY FACULTY OF SCIENCE DEPARTMENT OF MATHEMATICS	
	EXAMINATION FOR SENIORS (LEVEL THREE) STUDENTS OF COMPUTER SCIENSE	
	COURSE TITLE: COMPUTER ORGANIZATION &ASSEMBLY LANGUAGE PROGRAMMING	COURSE CODE: CS3101
DATE: 27-12-2022 | TERM: FIRST	TOTAL ASSESSMENT MARKS: 150	TIME ALLOWED: 2 HOURS

الاختبار من ٥ ورقات

Answer the Following Questions:

QUESTION 1: [Total marks: 41]

1. Define with draw (if any) each of the following: (15 marks)
   a. The basic four functions that the computer can perform.
   b. The main four structural components of computer.
   c. The major four structural components of CPU.
2. What are significant obstacles that you can met if you increase clock speed and logic density in the CPU? (5 marks)
3. What are the similarities and differences among symmetric multiprocessor, nonuniform memory access, and clusters? (6 marks)
4. Define with draw the concept of pipeline. (15 marks)
   Assume that: we need to execute the two instructions:

   Ins1: Load rA ← M, Ins2: Store M ← rB.

   By 4-stage processor (F: fetch, R: read, E: execute, and W: store).
   What is the total time in cycles of execution in:
   - Case1: without pipeline,
   - Case2: with pipeline?

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QUESTION 2: [Total marks: 35]

1. What are the main trends in hardware technology? (5 marks)
2. What are the two kinds of parallelism in applications? Discuss the four major ways that the computer hardware can exploit these two kinds of application parallelism. (10 marks)
3. Discuss the three main characteristics of a microprocessor. Explain the two main categories of microprocessor according to its instruction set. (10 marks)
4. Explain the three mapping functions used for mapping main memory blocks into cache lines. Highlight for each its main advantage and disadvantage. (10 marks)

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تابع الاختبار

QUESTION 3: [Total marks: 60]

Choose the best answer for each of the following points:

1. Which of the following is true about arithmetic pipeline?
   I. They are used to implement floating-point operations.
   II. They divide the floating-point operation into various sub problems
   III. They execute each sub problem in pipeline segment.
   A. I and II only B. I and III only C. II and III only D. I, II, and III.
2. Using multiple processors on the same chip, with a large shared cache, is called:
   A. Multicores. B. MIC. C. GPU. D. GPGPU.
3. There are difficulties that will prevent the instruction pipeline from operating at the maximum rate. These difficulties include:
   I. Different segments may take different times to operate on the incoming information.
   II. Two or more segments may require memory access at the same time, causing one segment to wait until another is finished with the memory.
   III. Different segments take the same time to operate on the incoming information.
   A. I and II only B. I and III only C. II and III only D. I, II, and III.
4. Using multiple cores on the same chip and developing software that can exploit this large number of cores, is called:
   A. Multicores. B. MIC. C. GPU. D. GPGPU.
5. Using cores to perform parallel operations on graphics data and process video, is called:
   A. Multicores. B. MIC. C. GPU. D. GPGPU.
6. When the same instruction is executed by uniprocessor using single data item, this category is called:
   A. MIMD. B. SISD. C. SIMD. D. MISD.
7. When the same instruction is executed by multiple processors using different data items, this category is called:
   A. MIMD. B. SISD. C. SIMD. D. MISD.
8. Architectural attributes of computer design include:
   A. Instruction set. B. Control signal. C. Memory technology used. D. All the above.
9. Which of the following is true about computer architecture?
   I. refers to the attributes of a system that are visible to a programmer.
   II. refers to the attributes that have a direct impact on the logical execution of a program.
   III. refers to the operational units and their interconnections that realize the architectural specifications.
   A. I and II only B. I and III only C. II and III only D. I, II, and III

تابع الاختبار

10. Which of the following is true about computer organization?
    I. Includes hardware details that are transparent to the programmer.
    II. refers to the attributes that have a direct impact on the logical execution of a program.
    III. refers to the operational units and their interconnections that realize the architectural specifications.

A. I and II only B. I and III only C. II and III only D. I, II, and III

11. When different instructions are executed by multiple processors using single data item, this category is called:

A. MIMD. B. SISD. C. SIMD. D. MISD.

12. Architectural attributes of computer design include:

A. Instruction set. B. Number of bits used to represent various data types.
C. I/O mechanisms. D. All the above.

13. Architectural attributes of computer design include:

A. Instruction set. B. Techniques for addressing memory.
C. I/O mechanisms. D. All the above.

14. Architectural attributes of computer design include:

A. Control signal. B. Interfaces between the computer and peripherals.
C. Memory technology used. D. None of the above.

15. Organizational attributes of computer design include:

A. Control signal. B. Interfaces between the computer and peripherals.
C. Memory technology used. D. All the above.

16. Organizational attributes of computer design include:

A. Control signal. B. Techniques for addressing memory.
C. I/O mechanisms. D. All the above.

17. Which of the following is true in the distinction between architecture and organization?
    I. Family of computer models can be introduced with the same architecture but with differences in their organization.
    II. Different models in this family have different price and performance characteristics.
    III. A particular architecture may exist many years and include several different computer models, its organization changing with changing technology

A. I and II only B. I and III only C. II and III only D. I, II, and III

18. For data exchanging with memory, CPU typically uses:

A. Two internal registers: memory address register and memory buffer register.
B. Two external registers: I/O address register and I/O buffer register.
C. Three internal registers: instruction register, data register, and control register.
D. Three external registers: instruction register, data register, and control register.

تابع الاختبار

19. Which of the following is the role of MAR (memory address register)?
    A. Specifies a particular I/O device.
    B. Contains the data to be written into memory or receives the data read from memory.
    C. Specifies the address in memory for the next read or write.
    D. Used for the exchange of data between an I/O module and the CPU.
20. Which of the following is the role of MBR (memory buffer register)?
    A. Specifies a particular I/O device.
    B. Contains the data to be written into memory or receives the data read from memory.
    C. Specifies the address in memory for the next read or write.
    D. Used for the exchange of data between an I/O module and the CPU.
21. Which of the following is the role of I/OAR (I/O address register)?
    A. Specifies a particular I/O device.
    B. Contains the data to be written into memory or receives the data read from memory.
    C. Specifies the address in memory for the next read or write.
    D. Used for the exchange of data between an I/O module and the CPU.
22. Which of the following is the role of I/OBR (I/O buffer register)?
    A. Specifies a particular I/O device.
    B. Contains the data to be written into memory or receives the data read from memory.
    C. Specifies the address in memory for the next read or write.
    D. Used for the exchange of data between an I/O module and the CPU.
23. Assume that: two devices A and B are connected on the bus, they send data on the bus at the same time, their signals will:
    A. Successfully transmit.
    B. Overlap and become garbled.
    B. One signal is transmitted and the other ignored.
    D. none of the above.
24. Assume that: we have two buses: A: one line bus and B: eight lines bus. Th 8-bit unit of data can be transmitted:
    A. Over A parallel and over B in sequence of eight digits.
    B. Over A in sequence of eight digits and over B parallel.
    C. Over A and B parallel.
    D. Over A and B in sequence of eight digits
25. When the processor executes instructions that may not be needed, this is called:
    A. Branch prediction. B. Pipelining. C. Parallelism. D. Speculative execution.
26. Which of the following is good approach to increase the processor speed?
    A. Increase the hardware speed of the processor.
    B. Increase the size and speed of caches that are interposed between the processor and main memory.
    C. Make changes to the processor organization and architecture that increase the effective speed of instruction execution.
    D. All the above.

27. Which of the following is true about memory module?

I. It consists of a set of locations defined by sequentially numbered addresses.
II. Each location contains a binary number that can be interpreted as either an instruction or data.
III. Each location contains a binary number that is interpreted as data only.

A. I and II only. B. I and III only. C. II and III only. D. I, II, and III

28. The key characteristics of computer memory include:

A. Location. B. Capacity. C. Unit of transfer. D. All the above.

29. There is a trade-off among the three key characteristics of memory. Which of the following relationships are hold?

A. Faster access time, greater cost per bit. B. Greater capacity, slower access time.
C. Smaller capacity, faster access time. D. All the above.

30. Method of accessing units of data in memory include:

A. Sequential access. B. Random access. C. Associative access. D. All the above.

QUESTION 4: [Total marks: 14]

For each of the following sentences, determine whether it is true or false:

1. When different instructions are executed by multiple processors using different data items, this category is called MIMD.
2. In general, MIMD is more flexible and thus more generally applicable than SIMD, but it is inherently more expensive than SIMD.
3. In non-volatile memory, information is lost when electrical power is switched off.
4. Physical cache (known as a virtual cache) stores data using virtual addresses. The processor accesses the cache directly, without going through the MMU.
5. The large caches tend to be slightly slower than small ones.
6. Using applications are supported by combination between CPU and GPU, is called GPGPU.
7. The concept of memory cycle time is primarily applied to random-access memory.

End of examination

EXAMINERS	**DR. MOUSAAD WAGEH HASSAN**	**DR/**
	DR.	**DR/**

With best wishes

TANTA UNIVERSITY
FACULTY OF SCIENCE
DEPARTMENT OF MATHEMATICS

EXAMINATION FOR (LEVEL THREE) STUDENTS OF COMPUTER SCIENSE

COURSE TITLE: DESIGN & ANALYSIS OF ALGORITHMS	COURSE CODE: CS3103
DATE: 1-1-2023	TOTAL ASSESSMENT MARKS: 150	TIME ALLOWED: 2 HOURS

Answer the Following Questions:

الاختبار من ٤ ورقات

These figures are required for Questions

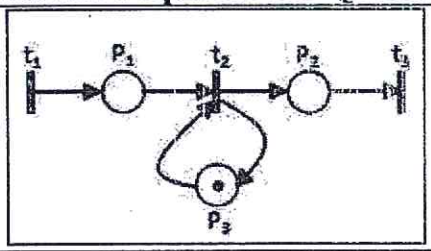

Fig. 1

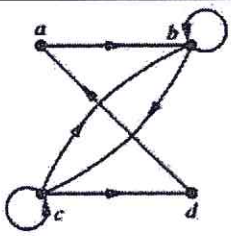

Fig. 2

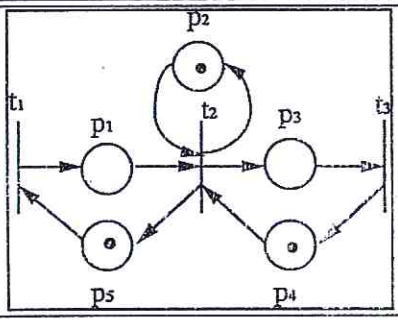

Fig. 3

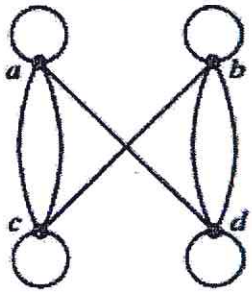

Fig. 4

QUESTION 1: [Total marks: 36]

1. Discuss the safeness of PN of Fig. 1 and if it is not satisfied make suitable modifications to convert it to be safe PN. (10 marks)
2. For the graph of Fig. 2 find **walk, trail, path, circuit,** and **cycle.** (10 marks)
3. Define the algorithm and the three ways used to represent the algorithm. (6 marks)
4. Rearrange, in ascending order, the array A = ⟨75, 18, 40, 5, 10, 65, 5, 14, 15, 3, 11⟩ using the insertion sort algorithm. (10 marks)

QUESTION 2: [Total marks: 40]

1. Draw the graph represented by the following adjacency matrix and determine its type. (7 marks)

$$\begin{array}{c} \\ a \\ b \\ c \\ d \end{array}\begin{array}{c} \begin{array}{cccc} a & b & c & d \end{array} \\ \begin{bmatrix} 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 \end{bmatrix} \end{array}$$

2. Define the following: Petri net structure, Petri net graph, enabling rule, and firing rule. (8 marks)
3. For the graph of Fig. 4 find: (10 marks)
   a. Adjacency matrix. b. Incidence matrix.

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4. Consider the PN of Fig. 3: (15 marks)
   a. Find reachability graph, RS, and sequence of firing of transitions
   b. Discuss the deadlock for it.

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QUESTION 3: [Total marks: 54]

Choose the best answer for each of the following points.

1. In Petri nets, the tokens are represented by:
   A. Arrows. B. Bars. C. Circles. D. Small dots
2. Adjacency matrix of a graph with n vertices is based on the ordering of these vertices. So, there are:
   A. n! different adjacency matrices. B. 2^n different adjacency matrices.
   C. n^2 different adjacency matrices. D. n different adjacency matrices.
3. Multiple edges are represented in the incidence matrix using:
   A. Rows with entries that are all zeros. B. Columns with identical entries.
   B. Columns with entries that are all zeros. D. Rows with identical entries.
4. The size of a graph is the number of:
   A. Edges. B. Vertices. C. Subgraphs. D. Components.
5. The RAM model contains instructions that takes a constant amount of time such as:
   A. Arithmetic. B. Data movement. C. Control. D. All the above.
6. A graph $G = (V, E)$ with $V = \emptyset$ is called:
   A. Null graph. B. Trivial graph. C. Empty graph. D. Multi graph.
7. If the two vertices u and v are endpoints of an edge e, then they called:
   A. Parallel. B. Isolated. C. Pendant. D. Adjacent.
8. The edges that have the same end vertices are called:
   A. Parallel. B. Isolated. C. Pendant. D. Adjacent.
9. Multiple edges connecting the same pair of vertices v_i and v_j, or multiple loops at the same vertex make the adjacency matrix:
   A. Not zero–one matrix. B. Zero-one matrix
   C. Contain no zeros. D. contain no ones.
10. Adjacency matrix can represent:
   A. Simple undirected graph only. B. Multigraph permitting loops only.
   C. Digraph only. D. All the above.
11. In Petri nets, the places are represented by:
   A. Arrows. B. Bars. C. Circles. D. Small dots

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12. Diagonal of adjacency matrix is all 0, in zero-one matrix, if the graph is:

A. Simple with loops. B. Simple with no loops.

B. Multigraph permitting loops. D. All the above.

13. Non-zero entries in the diagonal of adjacency matrix mean that the graph:

A. Has not loop B. has parallel edges. C. Has loops. D. has not edges.

14. In analyzing algorithm when we consider the case that the maximum number of steps taken on any instance of size n, then the case called:

A. Best case. B. Average case. C. Worst case. D. None of the above.

15. A graph $G = (V, E)$ with $|V| = 1$ is called:

A. Null graph. B. Trivial graph. C. Empty graph. D. Multi graph.

16. The RAM model contains instructions that represent a gray area in RAM such as:

A. Shift left. B. Data movement. C. Control. D. All the above.

17. In Petri nets, the arcs are represented by:

A. Arrows. B. Bars. C. Circles. D. Small dots

18. Which of the following is true about tokens?

I. They used to indicate which places are active.

II. They are represented by small dot in the places.

III. Their number and their distribution determine the dynamic behavior of a Petri net.

A. I and II only. B. I and III only. C. II and III only. D. I, II, and III.

19. W_n, for $n \geq 3$, can be obtained by adding an additional vertex to:

A. C_n and connect this new vertex to each of the n vertices in C_n by new edges.

B. K_n and connect this new vertex to each of the n vertices in K_n by new edges.

C. Q_n and connect this new vertex to each of the n vertices in Q_n by new edges.

D. None of the above

20. The RAM model contains instructions that represent a gray area in RAM such as:

A. Exponentiation. B. Data movement. C. Control. D. All the above.

21. Loops are represented in incidence matrix using:

A. Diagonal with ones in some entries.

B. Diagonal with zeros in some entries.

C. A column with exactly one entry equal to 1.

D. A column with entries that are all zeros.

22. A graph $G = (V, E)$ with $E = \emptyset$ is called:

A. Null graph. B. Trivial graph. C. Empty graph. D. Multi graph.

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23. The edges that share a common end vertex are called:

A. Parallel. B. Isolated. C. Pendant. D. Adjacent.

24. The vertex whose degree is 1 is called:

A. Trivial. B. Isolated. C. Pendant. D. Adjacent.

25. The vertex whose degree is 0 is called:

A. Trivial. B. Isolated. C. Pendant. D. Adjacent.

26. The order of a graph is the number of:

A. Edges. B. Vertices. C. Subgraphs. D. Components.

27. In Petri nets, the transitions are represented by:

A. Arrows. B. Bars. C. Circles. D. Small dots

QUESTION 4: [Total marks: 20]

Each of the following sentences, determine whether it is true or false:

1. In an undirected simple graph of order n, the maximum degree of each vertex is n - 1 and the maximum size of the graph is $(n - 1)/2$.
2. Adjacency matrix of graph G is based on the ordering chosen for the vertices, so it is not unique.
3. Adjacency matrix of all undirected graphs is not necessarily symmetric.
4. The adjacency matrix for a directed graph does not have to be symmetric.
5. In Petri nets, arcs are allowed to connect two places or two transitions.
6. Running time of an algorithm is the number of primitive operations or steps executed.
7. An arc in Petri net always connects two places to a transition in either direction.
8. Analyzing an algorithm means predicting the resources that the algorithm requires such as memory and running time.
9. There is no upper limit to the number of arcs that can connect to a place or a transition.
10. In Q_n, two vertices are adjacent if and only if the bit strings that they represent differ in exactly one-bit position.

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End of examination

EXAMINERS	**DR. MOUSAAD WAGEH HASSAN**	**PRF.**
	DR.	**DR/**

With best wishes

	DEPARTMENT OF MATHEMATICS **TANTA UNIVE RSITY** **FACULTY OF SCIENCE** **(Computer Science Division)** **Final_- exam**		
	EXAMINATION FOR PROSPECTIVE STUDENTS (3RD YEAR)		
	COURSE TITLE: ***CONCEPT OF PROGRAMMING LANGUAGE***	**DATE: 15/1/2023**	**COURSE CODE: CS 3107**
	TIME ALLOWED: 2 H	**Total score: 150**	

Answer the following questions:

Question 1: Short Answer Questions (50 Marks: 10 for each pointe)

1. What is the output of the following Java program?

```
class increment {
    public static void main(String args[])
    {
        int g = 3;
        System.out.print(++g * 8);      }    }
```

2. What will the following code print?

```
for (int i = 10; i > 0; i--);

System.out.print(``Meow! ");
```

3. What is wrong in the following statements?
   (a) System.out.printf("%5d %d", 1, 2, 3);
   (b) System.out.printf("%5d %f", 1);
   (c) System.out.printf("%5d %f", 1, 2);
4. What is the Inheritance? Why is Inheritance used in Java?
5. What are the differences between the constructors and methods?

Question 2: MCQ (50 Marks: 5 for each pointe)

1. Which of the following is a superclass of every class in Java?
   a) ArrayList
   b) Abstract class
   c) Object class
   d) String
2. Which of the following statements is correct?
   a) Public method is accessible to all other classes in the hierarchy
   b) Public method is accessible only to subclasses of its parent class
   c) Public method can only be called by object of its class
   d) Public method can be accessed by calling object of the public class
3. Which of the following is a valid declaration of a char?

   a) char ch = '\utea';
   b) char ca = 'tea';
   c) char cr = \u0223;
   d) char cc = '\itea';

4. Which of the following for loop declaration is not valid?

   a) for (int i = 99; i >= 0; i / 9)
   b) for (int i = 7; i <= 77; i += 7)
   c) for (int i = 20; i >= 2; - -i)
   d) for (int i = 2; i <= 20; i = 2* i)

5. **The break statement in Java is used to ___.**

   a) Terminates from the loop immediately
   b) Terminates from the program immediately
   c) Skips the current iteration
   d) All of these

6. **Which of these is the correct method to create an array in java?**

   a) int[] arr = {1, 3, 5};
   b) arr = new int[] {3, 1, 8};
   c) int arr[] = {1, 4, 6};
   d) All of these

7. Which of these cannot be used for a variable name in Java?
   a) identifier & keyword
   b) identifier
   c) keyword
   d) none of the mentioned
8. What is not the use of "this" keyword in Java?
   a) Referring to the instance variable when a local variable has the same name
   b) Passing itself to the method of the same class
   c) Passing itself to another method
   d) Calling another constructor in constructor chaining
9. Which of these are selection statements in Java?
   a) break
   b) continue
   c) for()
   d) if()
10. Which of these is a non-access modifier?

    a) public
    b) private
    c) native
    d) All of these

Question 3: *TRUE or FALSE questions* **(50 Marks:** 5 for each pointe)

(1) We can pass objects to method arguments in Java.
(2) The Java program can accept input from the command line.
(3) We can have multiple classes in same java file.
(4) The default value of Boolean variable is true.
(5) Java identifiers can contain letters, digits, and the underscore symbol and may start with a digit.
(6) In a for loop header, for (initializer; condition; update), the Java compiler requires initializer to initialize a loop variable and update to update it.
(7) The object class is a superclass for all the classes in Java.
(8) Assignment operator is evaluated Left to Right.
(9) Java programming is not statically-typed, means all variables should not first be declared before they can be used.
(10) The modifiers public and static cannot written in either order "public static" or "static public".

EXAMINERS **DR/ FATMA SHABAAN**

With my best wishes

1969	Tanta University Faculty of Science Department of Mathematics		
	Final term exam for the summer semester 2022-2023		
	Course title:	Operations Research (1)	**Course code:** MA3103
	Date:5 /1/2023	Total Marks: 150	**Time allowed:** 2 Hours

Answer all the following questions:

First question:

(a) Prove that if a L.P.P. has at least two optimal feasible solutions, then there are infinite number of optimal solutions.

(b) Prove that the sum $S = S_1 + S_2$ of two convex sets S_1, S_2 in R^n is a convex set.

(c) Show that the set $S = \{x : x = (x_1, x_2) : x_1 \geq 2, \quad x_2 \leq 4\} \subset R^2$ is convex set?.

Second question:

(a) Solve graphically the following LPP:

$$\max z = 2x_1 + 3x_2 \quad s.t. \quad 3x_1 + x_2 \leq 1, \; 3x_1 + x_2 \leq 10, \quad x_1, x_2 \geq 0$$

(b) By Simplex method solve the following LPP:

$$\max z = x_1 - x_2 + 3x_3$$

$$s.t. \quad x_1 + x_2 + x_3 \leq 10; \; 2x_1 - x_3 \leq 3; \quad 2x_1 - 2x_2 + 3x_3 \leq 0; \; x_1, x_2, x_3 \geq 0.$$

Third question:

(a) State and prove the weak Duality theorem?

(b) Find the dual of the following L.P.P.

$\min z = x_1 + x_2 + x_3$ subject to

$x_1 - 3x_2 + 4x_3 = 5, \; x_1 - 2x_2 \leq 3, \; 2x_2 - x_3 \geq 4 \; x_1, x_2 \geq 0, x_3$ *is unrestricted in sign*

Fourth question:

(a) Write a short note on " Transportation problem"

(b) Determine an initial basic feasible solution to the following transportation problem using Vogel's approximation method (VAM).

	d_1	d_2	d_3	
S_1	x_{11} 2	x_{12} 7	x_{13} 4	5
S_2	x_{21} 3	x_{22} 3	x_{23} 1	8
S_3	x_{31} 5	x_{32} 4	x_{33} 7	7
S_4	x_{41} 1	x_{42} 6	x_{43} 2	14
	7	9	18	

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(c) Solve the following game to find the saddle point.

		Player B				
		b_1	b_2	b_3	b_4	b_5
Player A	a_1	4	0	1	7	−1
	a_2	0	−3	−5	−6	5
	a_3	3	2	2	4	3
	a_4	−6	1	−2	0	−5

Examiner:	Dr. N. El-Kholy

Tanta university - faculty of science Department of Mathematics		
Final Exam for the First Semester 2022-2023		
Course Title: MA3125	Abstract Algebra and Topology	
Date:22/1/2023	Computer Science Section	Time Allowed:2H

Answer the following questions:

Question 1: Choose the correct answer (40 Marks)

1)	$\tau = \{X, \varphi, \{a\}, \{b\}, \{a, b\}, \{a, c\}\}$ is not a topology on $X = \{a, b, c, d\}$ because			
a) $\{a, b, c\} \nsubseteq \tau$	b) $\{a\} \cup \{b\} \notin \tau$	c) $\{a, b, c\} \notin \tau$	d) $\{a, b\} \cap \{a, c\} \notin \tau$	
2)	In any topological space (X, τ) the set $\{p: \forall G \in \tau, p \in G, (G - \{p\}) \cap A \neq \varphi\}$ is called			
a) closure of A	b) limit points of A	c) interior of A	d) exterior of A	
3)	In any topological space (X, τ) the set $\overline{A} \cap \overline{(X - A)}$ is called			
a) boundary of A	b) interior of A	c) closure of A	d) exterior of A	
4)	In any topological space (X, τ) the closure of any subset $A \subseteq X$ equal			
a) $\overline{A} \cap A^o$	b) $A^b \cap A^o$	c) $A^b \cup A^o$	d) $\overline{A} - A^o$	
5)	..... is the biggest open set contained in the subset A.			
a) $\overline{A}$	b) A^b	c) A^{ex}	d) A^o	
6)	..... is the smallest closed set containing the subset A.			
a) $\overline{A}$	b) A^o	c) A^b	d) A^{ex}	
7)	The neighborhood system for any point $p \in X$ is equal $N_p = \{X\}$; in the case that the topological space (X, τ) is ..... space.			
a) closed	b) indiscrete	c) discrete	d) dense	
8)	The subfamily $\beta = \{X, \{a, b\}\}$ is **NOT** a base for the topology $\tau = \{X, \varphi, \{a, b\}, \{c, d\}\}$ on $X = \{a, b, c, d\}$ because			
a) $\{a, b\} \in \tau$ but it not be a union of members of β.	b) $\{c, d\} \in \tau$ and it a union of members of β.	c) $\{c, d\} \in \tau$ but it not be a union of members of β.	d) $\{a, b\} \in \tau$ and it a members of β.	
9)	The set $M = \{r + s\sqrt{17}: r, s \in Z\}$, with addition and multiplication of R is integral domain that have			
a) zero divisors	b) no zero divisors	c) no zeros	d) no inverse	
10)	An element $a \in R$ of a ring R is a divisor of an element $b \in R$ if there exists an element $c \in R$ such that			
a) $a \mid b.c$	b) $c = a.b$	c) $a = b.c$	d) $b = a.c$	
11)	In the usual topology the largest open set contained in [1,2]∪{4,5,6}is			
a) (1,2]	b) (1,2] ∪ {4,5,6}	c) (1,2)∪{4,5,6}	d) (1,2)	
12)	In topological spaces, the arbitrary intersection of open sets is			
a) always an open set	b) always a closed set	c) always a singleton set	d) not always an open set	

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13) In the usual topology, an open set can always be written as			
a) an arbitrary union of open intervals	b) an arbitrary intersection of open intervals	c) a finite union of open intervals	d) a finite intersection of closed intervals
14) In the ring (R,+, o) such that $a\ o\ b = a + \sqrt{2}b - 2$, the identity of this ring is equal			
a) $\sqrt{2}$	b) $2+\sqrt{2}$	c) $1+\sqrt{2}$	d) $1/\sqrt{2}$
15) The identity element for the binary operation * defined by $a * b = ab/5$, where a, b are the elements of a set of non-zero rational numbers, is			
a) $5/ab$	b) 0	c) 5	d) 1/5
16) The set $S = \{1, i, -i, -1\}$ with multiplication operation is			
a) semigroup	b) subgroup	c) monoid	d) abelian group
17) In the ring (R,+, o) the element $u \in R$ is the multiplicative identity of R if for any $a \in R$, ...			
a) $a+u=a$	b) $a\ o\ u = u$	c) $u\ o\ a = a$	d) $u+a=a$
18) A ring (R, *, +) is commutative if for any , $y \in R$, ...			
a) $x*y=y*x$	b) $x*y=y+x$	c) $x+y=y*x$	d) $x+y=y+x$
19) In the ring (P(X),Δ, ∩) the identity element is			
a) X	b) $\emptyset$	c) $P(X)$	d) $A \subset X$
20) In the ring (R,+, o) such that $a\ o\ b = a + \sqrt{2}b - 2$, the multiplicative inverse of $a \in R$ is			
a) $\sqrt{2}$	b) $2+\sqrt{2}-a$	c) $1+\sqrt{2}-a/\sqrt{2}$	d) $a/\sqrt{2}+\sqrt{2}$

Question 2: (60 Points)

a) Consider the function $f: X \to Y$ from X to Y and suppose τ is a topology on Y. Prove that $\tau^* = \{G \subseteq X: G = f^{-1}(U), U \in \tau\}$ is a topology on X.

b) Consider the topology $\tau = \{X, \varphi, \{a\}, \{b\}, \{a,b\}, \{a,b,c\}\}$ on $X = \{a,b,c,d,e\}$, Find $A^0, \overline{A}, A^{ex}, A^b, A'$ for the subset $A = \{a,d,e\}$.

c) Prove that the algebraic system $(P(X), \Delta, \cap)$ is a Boolean ring where Δ, is the symmetric difference of sets.

d) Prove that the set $S = \{x + y\sqrt[3]{3} + z\sqrt[3]{9}: x, y, z \in \mathbb{Q}\}$, is a ring with respect to addition and multiplication on $\mathcal{R}$.

With best wishes
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